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Dependence of the capacitance of trap states at the oxide–semiconductor interface on the interface trap density in nanoscale silicon-on-insulator FinFET transistors and its effect on electrophysical parameters

Mirzabahrom Foziljonov[1], Nuritdin Yunusaliyev[1*], Biloliddin Ergashev[2], Oybek Muminov[1], Gaybullo Tojiboyev[1]

[1] Faculty of Physics, Mathematics and Information Technology, Andijan State University, 170100 Andijan, Uzbekistan
[2] Faculty of Natural Sciences, Andijan State Pedagogical Institute, 170100 Andijan, Uzbekistan
* Corresponding author's e-mail: nyunusaliyev1997@gmail.com

ABSTRACT

In this scientific research work, the dependence of the capacitance of trap states at the oxide–semiconductor interface (C_{it}) on the interface trap density (D_{it}) in nano-scale SOI FinFET transistors, as well as its effect on the main electrophysical parameters of the device, was systematically studied. The modeling was carried out on the basis of the drift–diffusion transport model, and quantum corrections based on the density gradient approach were applied to take into account quantum effects at the nanometer scale. The mobility model, the dependence on impurity atom concentration, and the velocity saturation effect occurring under strong electric fields were taken into consideration. The capacitance of trap states at the oxide–semiconductor interface was evaluated based on the relation $C_{it} = q^2 D_{it}$, and its effects on the electrostatic field potential, charge carrier concentration, the subthreshold slope (SS) of the current–voltage characteristic, threshold voltage (V_{th}), and current–voltage characteristics were comprehensively analyzed. The results show that, with an increase in the interface trap density, an increase in C_{it} is observed, which reduces the electrostatic control of the gate over the channel. As a consequence, the sensitivity of the electrostatic field potential to the gate voltage decreases, the charge carrier concentration along the channel decreases, and the subthreshold regime characteristics deteriorate. The obtained results show that the quality of the oxide–semiconductor interface in nano-scale SOI FinFET transistors is one of the main factors determining the operating characteristics of the device, and they justify the necessity of controlling surface states in the design of high-performance nanoelectronic devices.

Keywords: SOI FinFET, interface trap capacitance, interface trap density, surface charge potential, subthreshold slope, threshold voltage, drift–diffusion model.

INTRODUCTION

The rapid progress in the field of modern nanoelectronics requires reducing the geometric dimensions of semiconductor devices down to the nanometer scale. However, the transition to such a scale gives rise to a number of complex problems in transistors, including the intensification of short-channel effects, an increase in leakage currents, variation in threshold voltage, and deterioration of the electrostatic control of the gate over the channel [1]. In this regard, the need for new structural solutions capable of providing a high level of electrostatic control is increasing. As one of the most promising practical directions, multi-gate transistor structures, in particular FinFET structures based on SOI technology, are being widely used and are playing an

important role in improving the performance of nanoscale devices [2].

In SOI-based FinFET transistors, as a result of the channel region being surrounded by the gate from several sides, the subthreshold characteristics are significantly improved, leakage currents are reduced, and the overall stability of the device is enhanced [3]. At the same time, in nanoscale structures, the quality of the interface region remains a decisive factor. In particular, defects and trap states present at the oxide–semiconductor interface significantly affects the electrophysical properties of the device [4]. As the interface trap density (D_{it}) increases, the number of energetic states capable of trapping charge carriers at the interface increases, which leads to changes in electrostatic control processes as well as in the transport characteristics of charge carriers [5].

One of the important properties of interface states is their capacitive response. This response is expressed through the capacitance of trap states at the oxide–semiconductor interface (interface trap capacitance), C_{it}. The capacitance of interface traps, describing the variation of the charge trapped in the trap with respect to potential, is considered a key parameter directly related to the interface trap density [6]. The capacitance of interface traps is determined by the following relation:

$$C_{it} = q^2 D_{it} \tag{1}$$

This expression shows that, as the interface trap density increases, the capacitance of interface traps also increases. As a result, a portion of the gate voltage is spent not on controlling the channel, but on balancing the charges trapped in the traps. This reduces the sensitivity of the channel surface potential to the gate voltage and leads to the degradation of the subthreshold regime [7].

In the subthreshold regime, the drain current depends exponentially on the electrostatic potential at the channel surface, and changes in the capacitance of trap states at the oxide–semiconductor interface produce the most significant effect precisely in this regime. An increase in the capacitance of traps at the oxide–semiconductor interface causes the degradation of subthreshold slope (SS), that is, the deterioration of the control characteristics of the transistor in the subthreshold region [8]. At the same time, traps located at the interface can also alter the charge distribution along the channel, electron concentration, current–voltage characteristics, and threshold voltage.

In existing scientific studies, the effects of the interface trap density (D_{it}) on threshold voltage, subthreshold slope, or current–voltage characteristics have often been investigated separately [9,10]. However, a comprehensive analysis of the capacitance of trap states at the oxide–semiconductor interface (C_{it}) in relation to these parameters has not been sufficiently covered. In particular, based on the dependence of C_{it} on D_{it}, a systematic study within a unified model of the interaction among electrostatic field potential, charge carrier concentration, the I_d–V_g characteristic, *SS*, and threshold voltage is an important task from both scientific and practical points of view. Accordingly, the main objective of this research is to determine the dependence of the capacitance of trap states at the oxide–semiconductor interface on the interface trap density in nanoscale SOI FinFET transistors and to comprehensively analyze its effects on the electrostatic field potential, charge carrier concentration, SS, threshold voltage, and current voltage characteristics. Unlike previous studies, which mainly investigated individual electrical parameters separately, this work presents a unified electrostatic framework that correlates the interface trap capacitance (C_{it}) with surface potential (φ_s), carrier concentration, subthreshold swing, threshold voltage (V_{th}), and transfer characteristics (I_d–V_g) under identical interface trap density conditions. This integrated analysis provides a more comprehensive understanding of the electrostatic degradation mechanisms in nanoscale SOI FinFETs.

BACKGROUND

Nanoscale transistors, particularly the FinFET architecture, differ from conventional planar MOSFETs in that they provide a high level of electrostatic control, exhibit low leakage currents, and effectively suppress short-channel effects. For this reason, FinFET devices are widely used as the main active elements in modern integrated circuits. Research studies published in recent years have shown that the three-dimensional gate structure of FinFETs significantly strengthens electrostatic control over the channel [11]. However, along with such geometric advantages, an increase in the sensitivity of the device to the quality of the oxide–semiconductor interface and to defects present at the surface has also been observed [12]. In particular, it has

been emphasized that an increase in the number of traps formed at the oxide–semiconductor interface may adversely affect the electrophysical parameters of the device. Trap states formed at the oxide–semiconductor interface have the ability to capture and re-emit charge carriers, and they directly affect the threshold voltage, subthreshold regime, current–voltage characteristics, and reliability of the device. A number of studies have shown that these states can reduce the electrostatic control of the gate over the channel, and that the interface trap density (D_{it}) can be evaluated based on variations in the threshold current [13]. Also, in the classical MOS theory developed by Chenming Hu, it was noted that the presence of surface states and charges trapped in the oxide can degrade the flat-band voltage (V_{fb}), threshold voltage, and current characteristics in the subthreshold region [14]. This once again confirms the importance of controlling the quality of the interface region in nanoscale transistors. In the literature, C_{it} is defined as the derivative of the charge charge captured by interface traps with respect to the electrostatic potential:

$$C_{it} = \frac{dQ_{it}}{d\varphi_s} \tag{2}$$

In the works carried out by Boksteen and co-authors, based on the functional relationship between the charge trapped in interface traps (Q_{it}) and the surface potential (φ_s), the concept of $C_{it}(\varphi_s)$ was introduced, and it was substantiated that this quantity is directly related to the subthreshold parameters. In particular, when the trap states formed at the interface are expressed in units of $cm^{-2}\cdot eV^{-1}$ with respect to energy, a linear dependence of the interface trap capacitance on the interface trap density is shown to be observed [15] (Figure 1).

In MOS structures, the total capacitance is not limited to the ideal oxide capacitance. In the works of Thomas and his co-authors, the equivalent circuit for a real MOSFET is analyzed in the following form:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{acc}+C_{dep}+C_{it}+C_{inv}} \tag{3}$$

Or, in the region where free charge carriers (electrons and holes) are almost absent, it simplifies to the following form:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}+C_{it}} \tag{4}$$

These expressions explain the change in the total gate-to-drain (source) capacitance with increasing C_{it}. In the literature, this very approach is considered one of the theoretical bases for determining D_{it} through C–V analysis [16]. The theory of the subthreshold slope is also closely related to the capacitance of interface traps. In the literature, the subthreshold slope is expressed by the following formula:

$$SS = ln(10)\frac{kT}{q}\left(1 + \frac{C_{dep}+C_{it}}{C_{ox}}\right) \tag{5}$$

This expression shows that, with an increase in C_{it}, SS also increases, that is, the subthreshold switching characteristics of the device deteriorate. In Boksteen's work, this relationship was written using the g_m/I_D method, and the following formula was used to evaluate C_{it} directly from SS [17]:

$$C_{it} = \left(\frac{SS}{u_T \ln(10)} - 1\right)C_{ins} \tag{6}$$

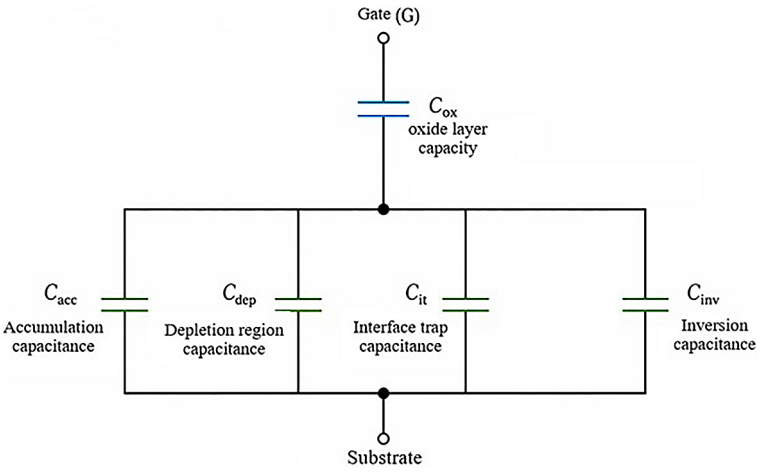

Figure 1. Equivalent capacitance scheme for real MOSFETs

where: $u_T = \frac{kT}{q}$, and this expression shows that the interface trap capacitance can be determined based on the subthreshold region parameters [18].

In studies conducted by Boksteen and his colleagues, it was shown that the interface trap density in interface trap states can be determined on the basis of the subthreshold current and the g_m/I_D method. In particular, the authors demonstrated that, for symmetrically fully depleted devices, the presence of interface traps increases the subthreshold ideality factor (body factor), m, above unity ($m > 1$). This indicates a deterioration of the gate electrostatic control caused by the additional capacitance associated with interface trap states, resulting in an increase in the minimum subthreshold swing. These results are of particular importance for FinFET devices fabricated on the basis of nanoscale SOI technology. This is because, at such a scale, the energy distribution of interface traps directly affects the electrostatic control of the gate over the channel as well as the formation of the subthreshold regime [19]. Traps present at the oxide–semiconductor interface also have a strong effect on the threshold voltage. In modern educational materials on the physics of the MOSCAP (metal–oxide–semiconductor capacitor), the threshold voltage for MOS structures is written as follows [20]:

$$V_{th} = V_{fb} + V_{ox} + \varphi_S \tag{7}$$

where: V_{fb} is the flat-band voltage (the gate voltage at which the energy bands at the semiconductor surface do not bend, that is, the field potential created by the charges in the traps is nearly equal to zero), V_{ox} is the voltage drop across the oxide layer, and φ_s is the potential at the semiconductor surface (the surface potential generated by the local charges located in the traps).

Therefore, an increase in the amount of charge Q_{it} accumulated in the interface traps leads to a shift in the flat-band voltage V_{fb}, which, in turn, causes a change in the value of the threshold voltage Vth. This shows that the effect of surface defects and trap states formed at the interface is not limited only to capacitance characteristics, but is also an important factor determining the threshold voltage, which is one of the main electrical parameters of the device [21]. Analyses related to the surface potential (φ_s) generated by the charges trapped in the traps at the oxide–semiconductor interface occupy an important place in studies carried out on MOS structures. In particular, in the theory of MOS capacitors, it is noted that the capacitance value is determined entirely by the surface-state potential, that is, the change in capacitance depends directly on the change in φ_s [22]. From this point of view, trap states at the interface affect the band bending and potential modulation at the channel surface, and as a result, these effects are reflected in the capacitance–voltage (C–V) and current–voltage (I_d–V_g) characteristics. In multi-gate transistors, particularly in FinFET structures, the sensitivity of the surface potential to the gate voltage is required to be high. However, an increase in the interface trap capacitance weakens this electrostatic advantage and reduces the efficiency of gate control over the channel.

Studies conducted in recent years confirm that interface traps are indeed one of the main limiting factors of the subthreshold regime. In particular, in studies carried out in 2025 on InGaAs-based nanosheet transistors, it was shown that the presence of trap states is directly related to the degradation of *SS*, and they were interpreted as an important factor limiting electrostatic control efficiency [23]. Despite the difference in material systems, these results reflect a general physical law for nanoscale field-effect transistors: unless interface trap states are sufficiently reduced, it will be difficult to achieve improvement in the electrophysical parameters of transistors. Nevertheless, in most of the existing scientific sources, the interrelations among the interface trap density (D_{it}), the interface trap capacitance, surface potential, SS, and threshold voltage have been analyzed mostly in terms of separate parameters. In particular, in nanoscale SOI FinFET transistors, a comprehensive study within a unified model of the interaction among surface potential, charge carrier concentration, the I_d–V_g characteristic, SS, and threshold voltage, based on the dependence of the capacitance of trap states at the oxide–semiconductor interface on the interface trap density, has not been sufficiently covered. Therefore, by selecting C_{it} as the central parameter, investigating its functional relationship with D_{it} and its influence on the main electrophysical characteristics of the device on the basis of an integrated model is regarded as a topical scientific issue.

RESEARCH METHODOLOGY

This research work was carried out on the basis of numerical modeling in the Synopsys Sentaurus TCAD software. As the object of the research, a vertical field-effect transistor fabricated on the basis of silicon technology, namely a FinFET structure, was selected. A three-dimensional geometric model of the device was developed, and its main geometric dimensions (the gate, channel, source and drain regions, as well as the oxide layers) were defined parametrically in a manner consistent with physically realistic conditions. The general view of the FinFET structure is presented in Figure 2, while the geometric dimensions of the transistor and the main technological parameters are shown in Table 1.

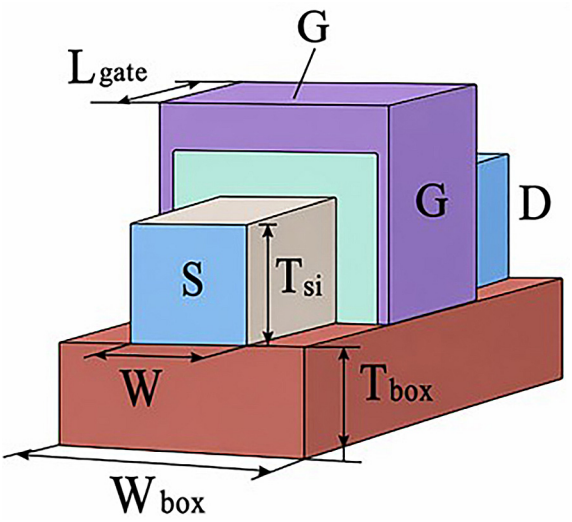

Figure 2. Structure of the modeled FinFET transistor

The SOI FinFET transistor was modeled on the basis of the drift–diffusion and thermodynamic transport models in order to select a transport model corresponding to the current–voltage characteristics of the SOI FinFET transistor [24]. According to the results presented in Figure 3, in the range of gate voltage up to approximately $V_g \approx$ 1 V, both I_d–V_g characteristics are almost identical.

Therefore, in order to save computational resources (power and time), charge carrier transport in the modeling process was described on the basis of the drift–diffusion model. In order to take quantum effects into account in nanoscale transistors, quantum corrections based on the density gradient approach were introduced. In addition, in the mobility model, the dependence on impurity atom concentration as well as the velocity saturation effect arising under strong electric fields were taken into account. In the calculations, the electrostatic state of the device and the distribution of charge carriers were determined by jointly solving the Poisson and continuity equations. The results of the model used in the simulations were compared with the experimental results presented in reference [25] by comparing the I_d–V_g characteristics (Figure 4). To further evaluate the reliability of the proposed TCAD model, a quantitative validation was performed using the subthreshold transfer characteristics, since this

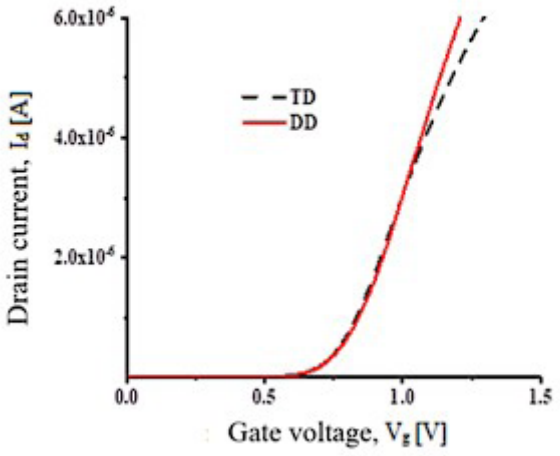

Figure 3. I_d–V_g characteristics modeled using the thermodynamic (TD) and drift–diffusion (DD) transport models

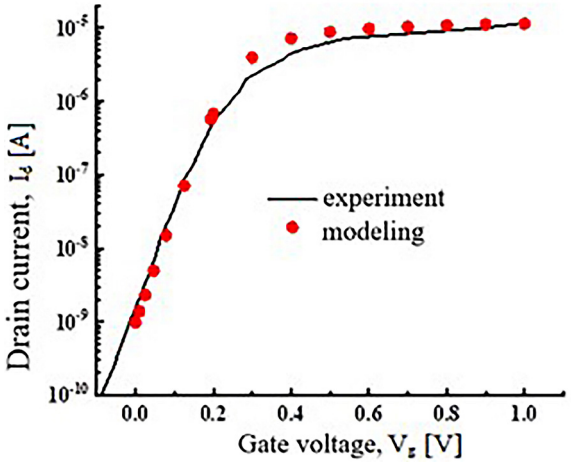

Figure 4. Calibration by modeling the I_d–V_g characteristics and comparing them with the experimental results presented in references

operating region is the most sensitive to interface trap effects and represents the primary focus of the present study. The comparison was intentionally limited to the subthreshold region because the investigated electrostatic parameters, including interface trap density (D_{it}), interface trap capacitance (C_{it}), surface potential (φ_s), subthreshold swing, and gate-control efficiency, predominantly govern the device behavior before strong inversion. Statistical evaluation based on the root-mean-square error (RMSE), average relative error, and coefficient of determination (R^2) confirmed a close agreement between the simulated and experimental characteristics. The obtained RMSE was 0.00939, the average prediction error remained below 3%, and the coefficient of determination ($R^2 = 0.995$) further verified the reliability of the proposed model. These results demonstrate that the developed TCAD model accurately reproduces the experimental electrostatic behavior within the subthreshold region and therefore provides a reliable basis for the subsequent investigation of interface-trap-induced degradation.

Within the framework of the study, in order to investigate the effect of interface trap states, a uniformly charged region model was applied at the oxide–semiconductor interface. In the present study, a spatially uniform interface trap density model was intentionally adopted to isolate the electrostatic influence of interface trap density on the device characteristics. The energy distribution of interface trap states and their dynamic capture/emission processes were not included because the objective of this work is to investigate the static electrostatic degradation induced by different interface trap densities under identical operating conditions. Accordingly, the calculated interface trap capacitance represents an equivalent electrostatic capacitance rather than a frequency-dependent dynamic trap response. Therefore, the proposed model is applicable to quasi-static electrostatic analysis of nanoscale SOI FinFETs. For different values of the interface trap density, the interface trap capacitance was calculated (Figure 5), and its effects on the electrostatic field potential, charge carrier concentration, the current–voltage (I_d–V_g) characteristic, *SS*, and threshold voltage were analyzed. In this way, based on the modeling results, the interrelation between the quality of the oxide–semiconductor interface and the electrophysical properties of the device was comprehensively evaluated. To ensure numerical reliability, a sufficiently refined finite-element mesh was employed in the HfO_2/Si interface region, the silicon channel, and the gate edges, where the strongest electrostatic field variations occur. Furthermore, adaptive bias stepping together with strict convergence criteria was applied throughout the simulations to obtain stable numerical solutions. The adopted numerical settings were verified to have a negligible influence on the calculated electrical characteristics compared with the variations induced by the investigated interface trap densities.

Table 1. Geometric dimensions of the transistor and its main parameters

Parameter name	Symbol	Modeling value
Doping concentration of Source, Drain, and Channel regions	N_{sub}	n-type (Phosphorus) 10^{20} cm^{-3}, p-type (Boron) 10^{20} cm^{-3}
Gate oxide thickness (HfO_2)	t_{ox}	2.5 nm
Channel thickness (Si)	T_{si}	30 nm
Channel width (Si)	T_{si}	12 nm
Buried oxide thickness (SiO_2)	T_{box}	100 nm
Gate length (metal)	L_{gate}	25 nm

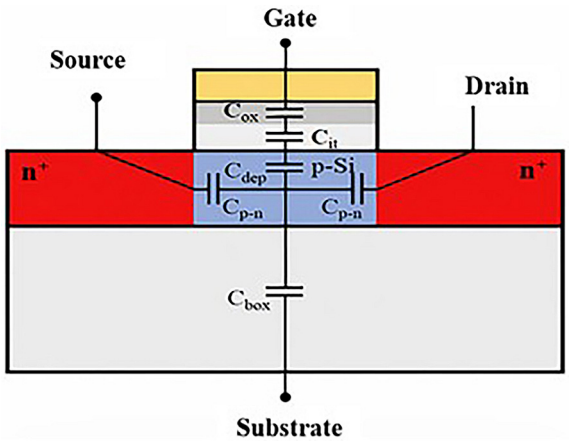

Figure 5. Equivalent capacitance model of the SOI MOSFET structure

RESULTS

The interface trap capacitance C_{it} formed at the oxide–semiconductor interface is the capacitive equivalent of the interface trap density D_{it} and describes the trapping and release of electric charges in the traps formed at the interface. The interface trap capacitance C_{it} is evaluated by expression (1).

As can be seen from Figure 6, at small values of D_{it} (10^8 – 10^{10} cm^{-2} eV^{-1}), the surface-state capacitance is negligible and changes very slowly. This indicates that, at low densities of surface states, the surface-state capacitance generated by the traps does not affect the total capacitance. Physically, in such a case, the capacitance of the gate–channel (gate–source (drain)) system is mainly determined by the oxide-layer capacitance C_{ox} and the depletion-layer capacitance C_{dep}. The surface-state capacitance generated by the interface traps is therefore almost unnoticeable. However, at values of D_{it} greater than 10^{11} cm^{-2}eV^{-1}, an increase in C_{it} is observed. In particular, in the range of 10^{12} – 10^{13} cm^{-2} eV^{-1}, the slope of the graph increases sharply, and we can observe a sharp increase in the surface-state capacitance of the interface traps. This shows that, at high densities of surface states, the interface traps participate in the charge exchange process and significantly affect the gate voltage.

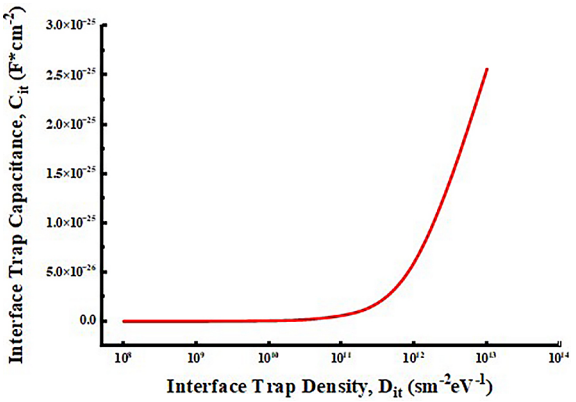

Figure 6. Effect of the interface trap density D_{it} on the interface trap capacitance Cit

This result means that, as the number of traps formed at the interface increases, a certain part of the gate voltage is spent not on controlling the channel, but on filling and balancing the interface traps with charge. This behavior is consistent with the equivalent-capacitance model of MOS structures reported in the literature, where interface traps act as an additional capacitive component that weakens the electrostatic coupling between the gate and the channel [26–28]. Therefore, an increase in C_{it} is considered one of the main factors reducing the efficiency of gate control. An increase in the surface-state capacitance directly affects the total capacitance of the device and its control through the electrostatic field. Through the surface-state potential generated by the charges located in the traps, it reduces the sensitivity to the gate voltage according to the following relation:

$$\frac{d\varphi_s}{dV_g} = \frac{C_{ox}}{C_{ox}+C_{dep}+C_{it}} \quad (8)$$

where: C_{ox} is the oxide-layer capacitance, C_{dep} is the depletion-layer capacitance and C_{it} is the capacitance generated by surface traps. It can be seen from this expression that, with an increase in C_{it}, the ratio $\frac{d\varphi_s}{dV_g}$ decreases.

Therefore, the increase in C_{it} observed in the figure is the main physical factor explaining the changes in the electrostatic field potential, electron concentration, *SS*, and threshold voltage in our subsequent results. The surface-state potential φ_s, generated by the charges trapped in the traps at the oxide–semiconductor interface, is the main parameter determining the variation of the overall electrostatic field potential at the channel surface. The surface-state potential φ_s characterizes the degree of channel control by the gate voltage. When traps are present in the interface region, a certain part of the gate voltage is spent not on bringing the channel into the inversion state, but on balancing the charges trapped in the traps. Therefore, an increase in the interface trap density D_{it} leads to a change in φ_s. The relationship

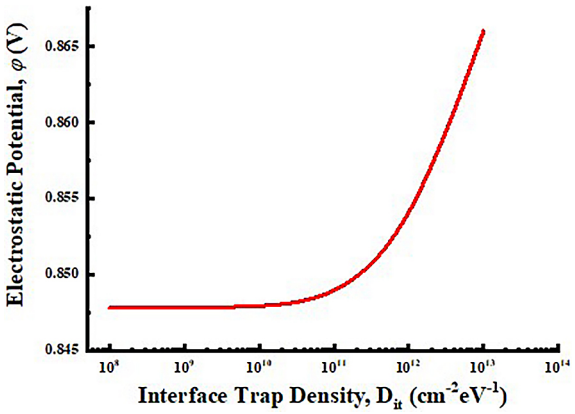

Figure 7. Effect of the interface trap density on the electrostatic field potential

between the gate voltage and the surface-state potential is expressed by Equation 8.

At D_{it} values of 10^8 – 10^{10} cm^{-2} eV^{-1}, the surface-state potential remains almost unchanged and stable. In this case, C_{it} is still very small, which indicates that the electrostatic control of the gate over the channel is strong. In other words, the electrostatic field potential at the channel surface is mainly determined by C_{ox} and C_{dep}. At D_{it} values higher than $10^{11} cm^{-2}$ eV^{-1}, the surface-state potential φ_s generated by the charges trapped in the interface traps begins to increase, and this increase becomes especially sharp in the range of 10^{12} – 10^{13} cm^{-2} eV^{-1}. This can also be seen in Figure 7. This result indicates the redistribution of charges in the traps at high densities of surface states and the appearance of an additional electrostatic potential at the channel surface. The important point here is that an increase in the value of the electrostatic field potential does not mean that the control of the gate over the channel has improved. On the contrary, as a result of the increase in the capacitance generated by the surface traps, the efficiency of the gate voltage in controlling the channel decreases, and the sensitivity of the electrostatic potential at the channel surface to the gate voltage weakens. The increase in the electrostatic field potential shown in Figure 7 indicates that it is influenced by the surface-state potential generated by the charges trapped in the traps. Physically, the increase in the electrostatic potential originates from the additional potential created by charges trapped at the HfO_2/Si interface rather than from improved gate control. As the interface trap capacitance (C_{it}) increases, a larger fraction of the applied gate voltage is consumed by charging the interface traps, thereby reducing the gate-to-channel electrostatic coupling. Consequently, although the absolute surface potential increases, its sensitivity to the applied gate voltage decreases, leading to the degradation of *SS*, threshold voltage, and carrier concentration. Let us now analyze the decrease in the concentration n of current-carrying charges in the channel under the effect of the trap-state capacitance C_{it}. The electron concentration n in the channel is the main electrophysical parameter representing the inversion state of the transistor. When the interface trap density increases, the increase in C_{it} generated by the interface traps changes the charge distribution in the channel and, as a result, significantly affects the concentration of free charge carriers. Therefore, analyzing the dependence of n on D_{it} is very important for explaining the physical significance of C_{it}. The following analysis refers to the quasi-static electrostatic response of the equivalent interface trap capacitance and does not include frequency-dependent trap dynamics. As can be seen from Equation 1, with an increase in D_{it}, C_{it} also increases. The increase in C_{it} creates an additional capacitance between the gate and the channel (Figure 5), and a portion of the gate voltage is spent not on creating the inversion state in the channel, but on filling the surface traps with charge. As a result, the generation of current-carrying charges inside the channel decreases.

This situation is expressed through the law of charge conservation as follows:

$$Q_{tot} = Q_{inv} + Q_{dep} + Q_{it} \tag{9}$$

where: Q_{tot} is the total charge present at the channel surface (the oxide–semiconductor interface), Q_{inv} is the current-carrying charge along the channel, Q_{dep} is the ionized charge in the semiconductor, and Q_{it} is the localized charge accumulated at the interface.

$$Q_{tot} = C_{ox}(V_g - \varphi_s) \tag{10}$$

Therefore, for the current-carrying charges along the channel, the following expression is obtained:

$$Q_{inv} = C_{ox}(V_g - \varphi_s) - Q_{dep} - Q_{it} \tag{11}$$

From this equation, it follows that, as Q_{it} increases, Q_{inv} decreases. Since the concentration of charge carriers depends on the inversion charge, an increase in C_{it} leads to a decrease in the number of charge carriers (Figure 8). As can be

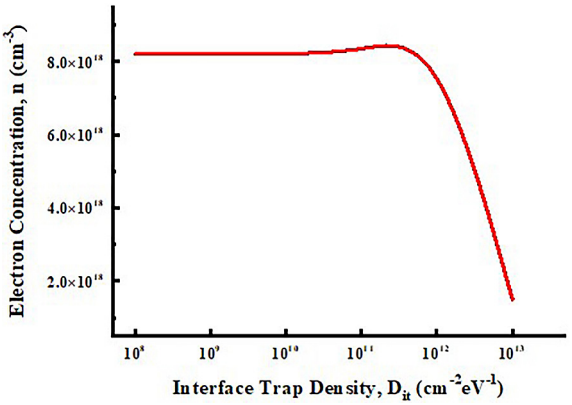

Figure 8. Effect of the interface trap density on electron concentration

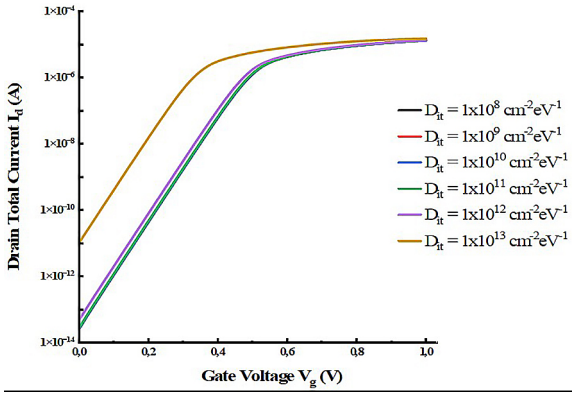

Figure 9. I_d–V_g characteristic obtained by modeling in the FinFET transistor for different values of D_{it}

seen from the graph, at low values of D_{it}, the concentration of current-carrying charges remains almost unchanged. This means that, within this range, C_{it} is still small relative to C_{ox} and C_{dep} and does not significantly hinder the inversion state of the channel. However, at high values of D_{it}, C_{it} increases significantly, and as a result, a decrease in the concentration of current-carrying charges is observed. The drain current–gate voltage characteristic, I_d–V_g, is one of the most important characteristics simultaneously representing the electrostatic and transport properties of the device. As C_{it} increases, channel control through the gate weakens, and as a result, the formation of the potential and inversion charges at the channel surface changes. Therefore, the I_d–V_g characteristic is considered one of the main indicators for evaluating the effect of C_{it} on device operation. In the subthreshold region, the drain current is exponentially related to the surface-state potential at the channel surface as follows:

$$I_d \infty \left(\frac{q\varphi_s}{kT}\right) \tag{12}$$

Thus, the response of the drain current to the gate voltage changes in accordance with the response of the surface-state potential at the channel surface to the gate voltage. When the interface trap capacitance C_{it} is present, the sensitivity of the surface-state potential to the gate voltage decreases according to equation (8). This shows that, with an increase in C_{it} in this equation, the efficiency of the gate voltage in controlling the channel decreases. As a result, in the subthreshold regime, the increase of current with respect to I_d–V_g slows down, and the slope of the I_d–V_g curve shifts to the left (Figure 9).

It can be concluded from Figure 9 that, at low values of D_{it}, the current–voltage curves are located very close to each other. This is explained by the fact that, at surface-state density values of 10^8 – 10^{10} cm^{-2} eV^{-1}, the value of C_{it} is still sufficiently small and does not create a significant additional capacitive load relative to the oxide-layer capacitance C_{ox}. In other words, within this range, the main part of the gate voltage is spent on forming the inversion layer in the channel region. As the value of D_{it} increases, C_{it} also increases correspondingly, and as a result, deformation is observed in the subthreshold part of the current–voltage curves. At high values of surface-state density (10^{12} – 10^{13}cm^{-2} eV^{-1}), the current–voltage characteristic plotted on a logarithmic scale takes on a "stretched" form, that is, the curve shifts to the left. This is explained by the fact that C_{it} weakens the electrostatic control of the gate over the channel and makes the formation of the inversion layer more difficult. A similar subthreshold-current degradation with increasing interface trap density has also been reported for nanoscale FinFET and MOSFET devices, confirming that the present simulation results are consistent with previously established electrostatic behavior [29–33]. The leftward shift observed at high values of D_{it} can be explained by the appearance of additional current mechanisms associated with interface trap states. Traps at the oxide–semiconductor interface temporarily capture charge carriers and then re-emit them, and as a result, in the subthreshold regime, additional trap-related currents I_{trap}, generated by the charges in the traps, appear in addition to the ideal diffusion current. The total current flowing from the drain varies according to Equation 13. Therefore, at large D_{it}, the transistor

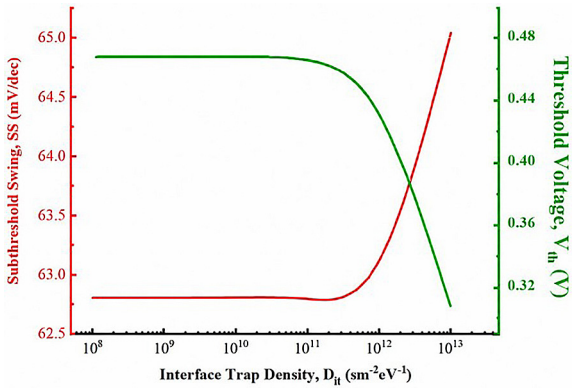

Figure 10. Effect of the interface trap density on *SS* (red curve, left axis) and threshold voltage (green curve, right axis)

begins to conduct current at relatively lower gate voltages. Within the framework of the adopted quasi-static electrostatic model, I_{trap} represents the equivalent contribution of interface-trap-assisted charge exchange rather than a time-dependent capture/emission current. That is, in the region near the threshold, the electrical response of the device changes under the influence of traps.

$$I_d = I_{diff} + I_{trap} \tag{13}$$

Another important aspect of the graph is that, at high gate voltages, the differences between the curves become negligible. This shows that, in the strong inversion state, the channel is filled with saturated charges and the relative effect of the traps gradually decreases. Thus, the main effect of C_{it} is manifested most pronounced in the subthreshold and near-threshold regions. This observation further confirms that interface trap capacitance is one of the dominant factors governing the electrostatic degradation of nanoscale SOI FinFETs under subthreshold operating conditions.

In FinFET transistors, the subthreshold slope (*SS*) is one of the main parameters for evaluating the quality of control in the subthreshold regime. It shows how much the gate voltage must change in order to change the drain current by one decade.

In other words, the smaller the *SS*, the more efficiently the transistor is controlled in the subthreshold regime. Therefore, analyzing how *SS* changes as a result of an increase in the interface trap density is very important for understanding the degradation of device electrostatics. Theoretically, *SS* is determined using Equation 5. It can be seen from this equation that, as the interface trap capacitance C_{it} increases, *SS* also increases. This is because C_{it} causes a portion of the gate voltage to be spent not on controlling the channel, but on filling the traps with charges.

Figure 10 simultaneously presents the variations of the subthreshold swing (SS, red curve, left vertical axis) and the threshold voltage (V_{th}, green curve, right vertical axis) as functions of the interface trap density (D_{it}). Presenting both parameters in a single figure enables a direct comparison of their correlated electrostatic behavior under increasing interface trap density. At low and intermediate values of D_{it}, both the red *SS* curve and the green V_{th} curve remain nearly constant, indicating that the interface trap capacitance (C_{it}) is still too small to noticeably affect the gate electrostatics. Consequently, the gate–channel coupling remains almost undisturbed, the *SS* stays close to its ideal value, and the threshold voltage exhibits only negligible variation. However, when D_{it} exceeds approximately 10^{11} $cm^{-2}eV^{-1}$, the red SS curve (left axis) gradually increases, whereas the green V_{th} curve (right axis) continuously decreases. These opposite trends originate from the same physical mechanism. As the interface trap capacitance increases, a progressively larger fraction of the applied gate voltage is consumed by charging the interface traps instead of controlling the inversion charge in the channel. As a result, the gate electrostatic control weakens, leading simultaneously to the degradation of the subthreshold swing and the reduction of the threshold voltage.

Therefore, the simultaneous evolution of the red SS curve and the green V_{th} curve confirms that the increase in interface trap capacitance (C_{it}) is the dominant electrostatic mechanism governing the degradation of nanoscale SOI FinFET performance.

CONCLUSIONS

In this scientific research work, the effect of the interface trap density D_{it} on the main electrophysical parameters of a nanoscale SOI FinFET transistor through the capacitance C_{it} generated by traps at the oxide–semiconductor interface was comprehensively analyzed. The obtained results showed that, with an increase in D_{it}, C_{it} also increases, and it is precisely this parameter that plays a central role in the weakening of the gate–channel coupling. An increase in the interface trap capacitance directs a portion of the gate voltage not to channel control, but to charge-exchange processes associated with the interface

states. According to the analysis results, as C_{it} increases, the variation of the surface-state potential generated by the charges trapped in the traps reduces the sensitivity of the gate voltage along the channel. As a result, the efficiency of controlling the channel state weakens and the formation of the inversion layer becomes more difficult. This was clearly manifested in the decrease in electron concentration, in the deformation of the current–voltage characteristic in the subthreshold region, and in the increase in *SS*. In particular, at high values of D_{it}, the rapid increase in C_{it} was found to lead to significant deterioration of the subthreshold regime. It was also shown that an increase in the interface trap capacitance affects the behavior of the threshold voltage and reduces the overall electrostatic stability of the device. In this sense, C_{it} appears not only as a capacitance quantity, but also as one of the main physical factors determining the electrostatic control, charge distribution, and transport regime of a nanoscale FinFET transistor. In general, the obtained results confirm that an increase in the interface trap capacitance leads to degradation of device parameters in nanoscale SOI FinFET transistors. Therefore, reducing the interface trap density and, accordingly, minimizing C_{it} is an important technological requirement for creating devices with high-quality and stable subthreshold characteristics.

REFERENCES

1. Frank D.J., Dennard R.H., Nowak E., Solomon P.M., Taur Y., Wong H.-S.P. Device scaling limits of Si MOSFETs and their application dependencies. Proc. IEEE. 2001; 89(3): 259–288. https://doi.org/10.1109/5.915374
2. Sun Y., Yu X., Zhang R., Chen B., Cheng R. The past and future of multi-gate field-effect transistors: Process challenges and reliability issues. J. Semicond. 2021; 42(2): 023102. https://doi.org/10.1088/1674-4926/42/2/023102
3. Lazzaz A., Bousbahi K., Ghamnia M. Performance analysis and optimization of 10 nm TG N- and P-channel SOI FinFETs for circuit applications. Facta Universitatis, Series: Electronics and Energetics. 2022; 35(4): 619–634. https://doi.org/10.2298/FUEE2204619L
4. Lü W., Zhang C., Chen D., Han Y., Wei W. Comparative study on random interface traps-induced reliability of NC-FinFETs and FinFETs. Silicon. 2023; 15: 4481–4488. https://doi.org/10.1007/s12633-023-02371-0
5. Zagni N., Caruso E., Puglisi F.M., Pavan P., Palestri P., Verzellesi G. Systematic modeling of electrostatics, transport, and statistical variability effects of interface traps in end-of-the-roadmap III–V MOSFETs. IEEE Trans. Electron Devices. 2020; 67(4): 1560–1566. https://doi.org/10.1109/TED.2020.2974966
6. Amir W., Shin J.-W., Shin K.-Y., Kim J.-M., Cho C.-Y., Park K.-H., Hoshi T., Tsutsumi T., Sugiyama H., Matsuzaki H., Kim T.-W. A quantitative approach for trap analysis between Al0.25Ga0.75N and GaN in high electron mobility transistors. Sci. Rep. 2021; 11: 22401. https://doi.org/10.1038/s41598-021-01768-4
7. Yu S., White M.H., Agarwal A.K. Experimental determination of interface trap density and fixed positive oxide charge in commercial 4H-SiC power MOSFETs. IEEE Access. 2021; 9: 149118–149124. https://doi.org/10.1109/ACCESS.2021.3124706
8. Yoon M. Subthreshold conduction of disordered ZnO-based thin-film transistors. Micromachines. 2023; 14(8): 1596. https://doi.org/10.3390/mi14081596
9. Mishra N.V., Medury A.S. Impact of band edge energy on interface traps and electrostatics of ultra-thin-body silicon-on-insulator devices. J. Appl. Phys. 2023; 133(17): 175702. https://doi.org/10.1063/5.0147578
10. Belkhiria M., Aouaini F., Aldaghfag S.A., Echouchene F., Belmabrouk H. Investigation of trap density effect in gate-all-around field effect transistors using the finite element method. Electronics. 2023; 12(17): 3673. https://doi.org/10.3390/electronics12173673
11. Reddy M.N., Panda D.K. A comprehensive review on FinFET in terms of its device structure and performance matrices. Silicon. 2022; 14: 12015–12030. https://doi.org/10.1007/s12633-022-01929-8
12. Agrwal P., Kumar A. Reliability investigation of interfacial defects in InGaAs-SOI-FinFET for high-performance applications. Indian J. Pure Appl. Phys. 2024; 62(11): 1004–1011. https://doi.org/10.56042/ijpap.v62i11.12442
13. Vermeer M.L., Hueting R.J.E., Pirro L., Hoentschel J., Schmitz J. Interface states characterization of UTB SOI MOSFETs from the subthreshold current. IEEE Trans. Electron Devices. 2021; 68(2): 497–502. https://doi.org/10.1109/TED.2020.3043223
14. Hu C.C. Modern Semiconductor Devices for Integrated Circuits. 1st ed. Prentice Hall, Upper Saddle River, NJ, USA; 2010. ISBN: 9780136085256.
15. Paul A., Tettamanzi G.C., Lee S., Mehrotra S.R., Colleart N., Biesemans S., Rogge S., Klimeck G. Interface trap density metrology from sub-threshold transport in highly scaled undoped Si n-FinFETs. J. Appl. Phys. 2011; 110: 124507. https://doi.

org/10.1063/1.3660697

16. Wang Z., Lin Z., Si M., Ye P.D. Characterization of interface and bulk traps in ultrathin atomic layer-deposited oxide semiconductor MOS capacitors with HfO2/In2O3 gate stack by C–V and conductance method. Front. Mater. 2022; 9: 850451. https://doi.org/10.3389/fmats.2022.850451
17. Boksteen B.K., Schmitz J., Hueting R.J.E. Interface trap density estimation in FinFETs using the gm/ID method in the subthreshold regime. IEEE Trans. Electron Devices. 2016; 63(5): 1814–1820. https://doi.org/10.1109/TED.2016.2539382
18. Mchedlidze T., Erben E. Characterization of ultrathin fully depleted silicon-on-insulator devices using subthreshold slope method. Phys. Status Solidi A. 2020; 217(24): 2000625. https://doi.org/10.1002/pssa.202000625
19. Schmitz J., Kaleli B., Kuipers P., van den Berg N., Smits S.M., Hueting R.J.E. Interface trap density estimation in FinFETs from the subthreshold current. In: Proceedings of the 2016 International Conference on Microelectronic Test Structures (ICMTS), Yokohama, Japan, 28–31 March 2016; pp. 164–167. https://doi.org/10.1109/ICMTS.2016.7476199
20. Taur Y., Ning T.H. Fundamentals of Modern VLSI Devices. 3rd ed. Cambridge University Press, Cambridge, UK; 2022. https://doi.org/10.1017/9781108847087
21. Saha P., Banerjee P., Dash D.K., Sarkar S.K. Interface trap charge induced threshold voltage modeling of WFE high-k SOI MOSFET. Silicon. 2020; 12: 2893–2900. https://doi.org/10.1007/s12633-020-00386-5
22. Rummel B.D., Dhar S., Kaplar R.J. The completed High-Low method for interface state analysis in MOS capacitors. J. Appl. Phys. 2026; 139(18): 185708. https://doi.org/10.1063/5.0305772
23. Balestra L., Di Stasi S., Gnani E., Reggiani S., Chen M.Y., Iwai H., Chang E.Y. Impact of interface traps on the subthreshold performance of InGaAs nanosheet transistors. Solid-State Electron. 2026; 231: 109265. https://doi.org/10.1016/j.sse.2025.109265
24. Atamuratov A.E., Jabbarova B.O., Khalilloev M.M., Rajapov D.R., Yusupov A., Chedjou J.C., Blugan G., Saidov K. Impact of source (drain) doping profiles and channel doping level on self-heating effect in FinFET. Micro Nanostruct. 2025; 197: 208015. https://doi.org/10.1016/j.micrna.2024.208015
25. Basker V.S., Standaert T., Kawasaki H., Yeh C.C., Maitra K., Yamashita T., Faltermeier J., Adhikari H., Jagannathan H., Wang J., et al. A 0.063 μm² FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch. In: Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 19–20. https://doi.org/10.1109/VLSIT.2010.5556135
26. Nicollian E.H., Goetzberger A. MOS conductance technique for measuring surface state parameters. Appl. Phys. Lett. 1965; 7(8): 216–219. https://doi.org/10.1063/1.1754385
27. Nicollian E.H., Goetzberger A. The Si–SiO_2 interface—Electrical properties as determined by the metal-insulator-silicon conductance technique. Bell Syst. Tech. J. 1967; 46(5): 1055–1133. https://doi.org/10.1002/j.1538-7305.1967.tb01727.x
28. Berglund C.N. Surface states at steam-grown silicon–silicon dioxide interfaces. IEEE Trans. Electron Devices. 1966; ED-13(10): 701–705. https://doi.org/10.1109/T-ED.1966.15827
29. Hong B.H., Cho N., Lee S.J., Yu Y.S., Choi L., Jung Y.C., Cho K.H., Yeo K.H., Kim D.-W., Jin G.Y., Oh K.S., Park D., Song S.-H., Rieh J.-S., Hwang S.W. Subthreshold degradation of gate-all-around silicon nanowire field-effect transistors: Effect of interface trap charge. IEEE Electron Device Letters. 2011; 32(9): 1179–1181. https://doi.org/10.1109/LED.2011.2159473
30. Atamuratov A., Karimov I., Foziljonov M., Abdikarimov A., Atamuratov O., Khalilloev M. Impacts of local oxide trapped charge on electrical and capacitance characteristics of SOI FinFET. East Eur. J. Phys. 2025; (3): 357–364. https://doi.org/10.26565/2312-4334-2025-3-36
31. Yang Y.L., Zhang W., Chen Y.L., Yeh W.K. Study on interfacial trap location induced subthreshold slope degradation extracted by random telegraph noise for high-k/metal gate FinFET devices. Microelectronics Reliability. 2020; 111: 113728. https://doi.org/10.1016/j.microrel.2020.113728
32. Abdikarimov A.E., Foziljonov M., Karimov I.N. Capacitance-Voltage Method for Detecting the Local Oxide Trapped Charge in SOI FinFET. In: Proceedings of the 2022 International Conference on Information Science and Communications Technologies (ICISCT), Tashkent, Uzbekistan, 2022; pp. 1–3. https://doi.org/10.1109/ICISCT55600.2022.10146967
33. Qiu Y., Wang R., Huang Q., Huang R. A comparative study on the impacts of interface traps on tunneling FET and MOSFET. IEEE Transactions on Electron Devices. 2014; 61(5): 1284–1291. https://doi.org/10.1109/TED.2014.2312330