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A High Gain Single Switch DC-DC Converter with Double Voltage Booster Switched Inductors

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ABSTRACT

The research for novel power conversion topologies and the development of cutting-edge power component technologies are driven by the demand for renewable and much more efficient electricity generation, delivery, and conversion. Simulation and analysis high voltage gain DC-DC converter with double voltage booster switched inductor are analyzed in this paper. Multilevel boost converter topologies recently reintroduced, are gaining popularity as a solution for industrial and transportation power systems because they enable the use of innovative, efficient, but relatively low voltage low-voltage devices at greater voltage and power levels. there is only one power switch on the converter that is planned here, three diodes, two capacitors, and two inductors to achieve ultra-high gain with better efficiency. High voltage gain, minimal switch stress, and the ability to lessen input-current ripple and capacitor voltage ripple are all benefits of the topology. When it switches complementary, the capacitors' ripple is reduced, which lowers the size requirement for the capacitors. A 12V, 500 watts prototype was analyzed, simulated and designed. at a duty cycle of 0.75 it is achieved high DC-DC gain i.e 19 and efficiency 93%. The practicality of the converter will be demonstrated by the close agreement between the analysis and simulation findings.

Keywords: multilevel converter; boost converter; DC-DC converter; high gain converters.

INTRODUCTION

To supply high DC voltage loads using available low-voltage photovoltaic sources, the conventional, well-known, non-isolated boost converter [1] is frequently employed in single and three-phase switching regulators. Their uses have recently extended to include high-voltage DC bus generation, High-voltage DC Transmission and green power generation and distribution. Alternative high gain DC-DC boost topologies are being sought after that enable downsizing, better efficiency and lower system costs have been compelled by the expansion of power conversion duties and more stringent criteria. Emerging wide bandgap SiC and GaN power devices, as well as developments in the fields of control, driver ICs, and passives, all assist such a search.

Other than conventional boost converter (BC), non-isolated boost topologies, such as different multilevel converters, have been taken into consideration in the literature. In [2] and [3], three-level BC topologies for single-phase PFC and three-phase rectifiers, respectively, were taken into consideration. DC-DC converters with four levels and one and two quadrants were presented in [4]. Although writers did not mention it, With the circuit's many beneficial boost capabilities, two quadrant converters would be combined to form single directional component. An examination and assessment of a two-switch boost rectifier operating in discontinuous conduction mode (DCM) in a three-phase system are presented in Paper [5]. Two-switch topology has less harmonic distortion than a three-phase DCM boost rectifier with a single switch. To lessen input current ripple and perhaps EMI, a new architecture for a three-stage step-up converter with coupled inductors is presented in [6].

Flying capacitor boost converter (FCBC) topology with a three-level variant is utilized in low-power PFC [7]. Initially designed for

high-power industrial applications in the few kV and MW power range, the flying capacitor multilevel boost topology is now used in a variety of applications. There are many applications today that leverage multilayer topologies. The active neutral-point-clamped five-level converter (ANPC5L) is analyzed in [8] concerning the decrease of total harmonic distortion in high-speed, high-power applications. A three-level zero voltage transition pulse width modulation (ZVT PWM) boost-converter for power factor correction converter) PFC is suggested in [9]. This given System functions as two ordinary boost-converters that are interleaved. For an active soft switching circuit, only one auxiliary switch is required. MPPT control is used in a three-phase PV system with TLBC, as shown in [10]. Experimental data using a 10000 W prototype with a 10000 Hz frequency show that TLBC minimizes reverse recovery loss in diodes. Power switches in the TLBC operate independently in this case.

Regarding two separated DC-DC converter possibilities for extra traction, the study [11] goes into considerable depth. The DC voltage is approximately 3000 Volts DC. In any of the topology under consideration, the TLBC module is succeeded by a HBZCS PWM converter. Since the TLBC's capacitors are a component of the HBZCS's resonant process, they should be fairly modest. There hasn't been any experimental validation of the analysis. The TLBC and auxiliary converter, however, are concluded by the authors to be HBZCS and cannot properly operate throughout the entire DC range. (2.2–4.0 kV) input voltage. This claim is disputed by additional in-depth investigation and application. Diode-clamped three-level inverter-based three-level converters were described in [12]. Three-level converters were created in a sizable family. However, the two-level topology illustrated in the paper TLBC must truly be categorized as such because the diode clamp is ineffective in one of the primary operational modes. As seen in [13], a two-stage TLBC is working in a photovoltaic energy-producing plant. Two phase-shifted PWM inverters are powered by the output of the TLBC. Multilevel BC that uses renewable energy is described in the paper [14]. DC-DC boost converters are referred to as interleaved designs by the paper's authors. The authors carefully investigate four and five-level converter is proposed with a range of power switch control strategies, including potential ZVS applications [15].

The utility-scale of photovoltaic energy stations with two-level design is highlighted by the study [16]. A one MW utility-scale system includes two 500 kilo-Watts three-level high gain DC converters. Grid-connected inverters effectively control grid disturbances while maximizing converter output power. With a 1050 V input voltage from independent PV panels, each converter runs. An inverter with two levels of output offers 690 V AC mains. Paper [17] displays that examination of the TLBC's two operating modes reveals various advantages compared to conventional BC. It has been shown that the TLBC's choke's size and power losses are less than the conventional BC ones. TLBC small-signal models for both modes operate in continuous conduction mode. This succinct analysis of literature connected to BC at various levels increased interest in these topologies as a result of their likely to perform better than conventional BC in high applications for high voltage and power. Due to the fact that the typical boost converter yields significant voltage gain at high duty cycle values, it is not appropriate for very high voltage gains. A greater duty cycle value exacerbates the issues with transient responsiveness [18].

Another drawback of the converter's operation at excessive duty cycle is that insufficient time is allowed for the transfer of the inductor and capacitor's stored energy for a diode with reverse recovery time [19]. Due to voltage dips across switches, capacitors, and inductors' equivalent series resistance, the conventional boost converter (CBC) is significantly reduced at larger duty ratios [20]. The efficiency of the converter is influenced by the quantity of the circuit's components, their conduction times, and the switching frequency [21].

The literature proposes a number of topologies for DC-DC converters with isolation utilizing high-frequency transformers. By increasing the transformer's turn ratio, high voltage gain can be attained, although doing so increases the converter's price, size, and weight. Additionally, transformers add non-idealities to the system. Current transient issues through the switch can occasionally be caused by the associated inductor's leakage inductance [22, 23]. A Multi Stage Boost Converter with switched inductor structure designed in [24]. Coupled inductors could produce high voltage gain, however a clamp circuit needs to be developed [25, 26]. Due to problems with reverse recovery and leakage inductance

if the energy stored in the leakage inductance is not adequately utilized, the converter efficiency might decline in the two-stage operation of the converters with connected inductor [27].

The DC-DC boost converter suggested in this study could be a feasible solution to such issues, where high-voltage gain and compact equipment are needed. The suggested converter has fewer components overall than several recently proposed high-voltage gain DC-DC converter designs [28–30].

The converter described in this paper offers a solution to this issue by proposing a new topology, enabling high-voltage gain with a smaller component count.

POWER CIRCUIT AND OPERATING MODES

Figure 1 shows the suggested converter of this work. It is constituted of Three diodes, two no. of capacitors, two no. of inductors, and one power MOSFET switch. The converter operates in two operational modes, called Modes 1 and 2, because there is only single switch. (One for switch is on another one when the switch is off). The proposed converter can drive a variety of resistive loads and operational mode is continuous conduction (CCM).

Mode 1 (when MOSFET switch is kept on)

The power MOSFET S_{W1} is turned on in this mode, which also causes the diode D_{S1} to become forward-biased and begin conducting. As a result, the inductor L_1 experiences a linear flow of current I_{L1}, causing it to store energy. Figure 2 illustrates this situation. Following the brief transient period, inductor L_2 is charged through capacitors C_1 by flowing the current I_{L2}. Figure 2 shows the I_{L1} and I_{L2} directions. Power diodes D_{S2} and D_{S3} are reverse biased and are not conducting as a result of the reverse voltage polarity being put across them. As a result, the current I_{L2} simultaneously charges the capacitor C_2 with the reverse voltage polarity. The algebraic summing of I_{L1} and I_{L2} results in the current that circulates through S_{W1}. voltage across C_1 is appear across the load.

The voltage appeared at magnetizing element L_1 i.e $V_{L1(on)}$ is equal to applied DC voltage V_{IN}:

$$V_{L1(on)} = V_{IN} \tag{1}$$

The voltage appeared at magnetizing element L_1 i.e $V_{L2(ON)}$ is equals to voltage i.e V_{C1} across capacitor C_1. Hence:

$$V_{L2(on)} = V_{C1} + V_{C2} \tag{2}$$

Mode 2 (when MOSFET switch is kept off)

The power MOSFET S_{W1} is turned off in this mode. Now the polarity of the both inductors are changed and the current direction remains same like Mode 1 operation of the converter by forward biasing the Diodes D_{S2} and D_{S3}. Status of diodes

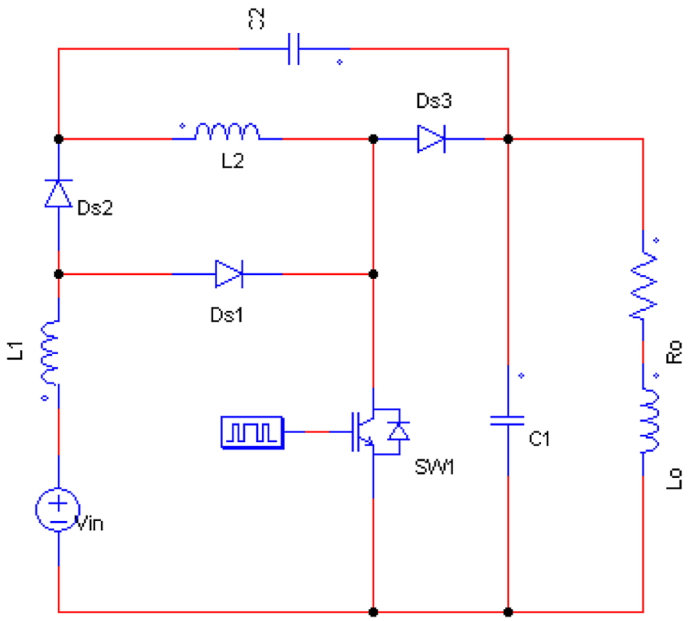

Figure 1. Proposed high voltage gain multi-level boost converter

D_{S2} and D_{S3} is indicated in Figure 3, and diode D_{S1} became open circuit.

The stored energy in the inductors discharged and transported towards the energy storage elements C_2 and C_1. The element C_1 is charged to a voltage V_{C1} i.e equal to the sum of voltage V_{IN}, V_{L1} and V_{L2}. the current flow direction is indicated in Figure 3. During this mode the voltage appeared across inductor L_1 i.e $V_{L1(OFF)}$ is the difference between input voltage i.e V_{IN} and capacitor voltages V_{C1} and $V_{C2.}$ this voltage can also be determined by difference between input voltage and voltage across inductor L_2 and output capacitor C_2, shown in Figure 3.

$$V_{L1(OFF)} = V_{IN} + V_{C2} - V_{C1} \tag{3}$$

or:

$$V_{L1(OFF)} = V_{IN} - V_{L2(OFF)} - V_{C1}$$

The voltage across L_2 i.e $V_{L2(OFF)}$, is equals to the voltage across capacitor C_2 i.e $V_{C2.}$ this can also find out by output voltage V_{OUT} minus input voltage V_{IN} and inductor L_1 voltage $V_{L(OFF)}$:

$$V_{L2(OFF)} = V_{C2} \tag{4}$$

from (1):

$$V_{IN} = L_1 \frac{dI_{L1}}{dt}$$

When power switch is in mode 1 i.e., MOSFET is kept on, the time difference dt equals T. Dy, where T is the switch S_{W1}'s switching time period and Dy is the duty-cycle.

$$V_{IN} = L_1 \frac{dI_{L1}}{Dy.T} \tag{5}$$

In further, from (3):

$$V_{IN} - (V_{C1} + V_{C2}) - L_1 \cdot \frac{dI_{L1}}{(1 - Dy) \cdot T} \tag{6}$$

STEADY-STATE ANALYSIS

Even when heavily loaded, the suggested converter continues to function in CCM mode. Assuming the suggested converter runs in CCM mode and that every implementation's components are ideal. Steady-state voltage gain, efficiency and voltage stresses across diodes and switches are represented here.

Steady-state voltage gain

Even with a high load, the suggested converter operates in CCM mode. The evaluation of the consistent voltage gain provided here is predicated on the premise that every element of the implementation is perfect and that it runs in CCM Mode. for the inductor L_1 volt-second balance applied. From the equations (5) and (6) results in:

$$V_{in} \cdot T \cdot Dy = -(V_{in} + V_{C2} - V_{C1})(1 - Dy) \cdot T$$

or:

$$V_{in} \cdot Dy = -(V_{in} + V_{C1} - V_{C2})(1 - Dy) \tag{7}$$

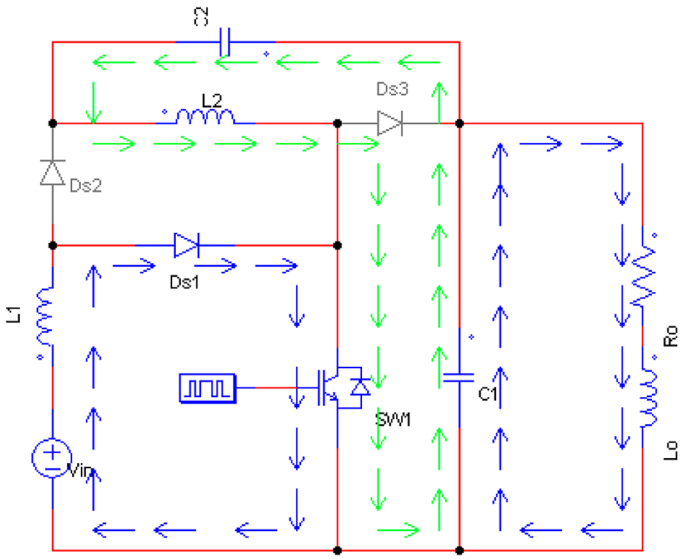

Figure 2. Mode 1 operation proposed high voltage gain multi-level boost converter

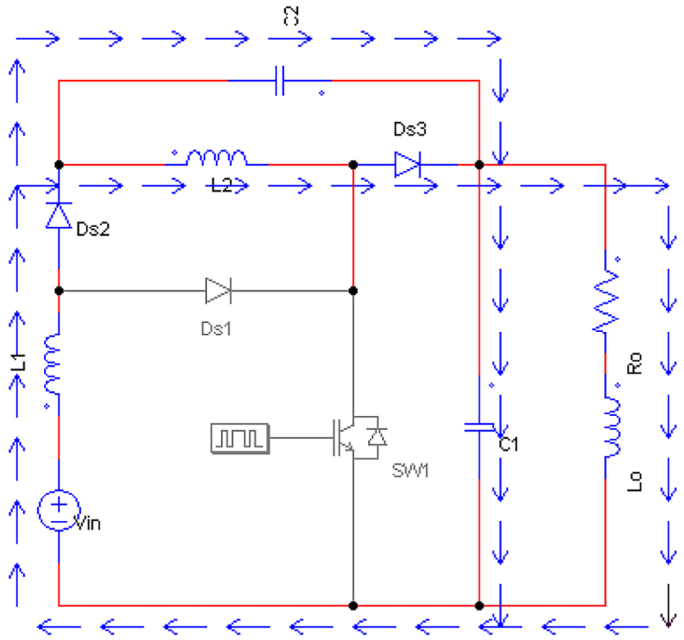

Figure 3. Mode 2 operation proposed high voltage gain multi-level boost converter

From Equation 2:

$$V_{C1} + V_{C2} = L_2 \frac{dI_{L2}}{1 - Dy} \tag{8}$$

From Equation 4:

$$V_{C1} = -L_2 \frac{dI_{L2}}{1 - Dy} \cdot \frac{1}{T} \tag{9}$$

for inductor L_2 volt-second balance applied. From the Equations 8 and 9 results in:

$$(V_{C1} + V_{C2}) \cdot Dy \cdot T = (-V_{C2}) \cdot (1 - Dy) \cdot T$$

It is clear from Figure 3 that the output voltage V_{OUT} and the voltage V_{C1} are equal. Consequently, V_{OUT} can be used in place of V_{C1} as the output voltage. This results in the equation shown below:

$$(V_{C1} + V_{C2}) \cdot Dy = (-V_{C2}) \cdot (1 - Dy) \tag{10}$$

By applying Equation 7, the voltage across C_2 may be derived from previous equation (10) in terms of input voltage V_{in} and duty cycle *Dy*, as shown below:

$$V_{C2} = V_{IN} \cdot \frac{1}{(1 - Dy)} \tag{11}$$

proposed converter steady-state voltage gain, G, maybe determined by altering the value of V_{C2} from (11) into (10), and is given by:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{1}{(1 - Dy)^2} \tag{12}$$

The converter's proposed voltage gain transfer function is in equation (12), showing that output voltage has an inverse relationship with one minus duty-cycle square. As a results, increasing the duty-cycle (*Dy*) value decrease the denominator value in equation (12) which increases the V_{OUT}. validating the proposed DC voltage boost converter's ability to boost voltage.

Efficiency analysis

Static loss and dynamic loss together make to the MOSFET's overall power loss. When the device is turned on, the MOSFET experiences static power loss because of the channel resistance. The switching of the device, however, results in dynamic power loss. You may determine the MOSFET's static power loss by using the formula:

$$P_{Sw,static} = r_{Ds(on)} \cdot I^2_{S(rms)} \tag{13}$$

In (13), $I_{S(rms)}$ is the rms current passing through the transistor, and $r_{Ds(on)}$ is the

transistor's on-state resistance. Dynamic loss is presented as for one switching period:

$$P_{Sw,dynamic} = \frac{V_{in} \cdot I_{out}}{3} \tag{14}$$

Consequently, the switch's overall power loss is given as:

$$P_{Sw,static} = r_{Ds(on)} \cdot I^2{}_{S(rms)} + \frac{V_{in} \cdot I_{out}}{3} \tag{15}$$

The power loss inside a diodes is the result of the combined power losses caused by the on-state resistance the forward bias and the forward voltage drop. Then, a diode's power loss can be expressed as:

$$P_D = V_F \cdot I_{D(avg)} + r_D \cdot I^2{}_{D(rms)} \tag{16}$$

In (16), $I_{D(avg)}$ represents the average current passing through the diode while it is turned on, while V_F represents the forward voltage drop of the diode and r_D represents the forward junction resistance. The power loss in a computer with capacitors can be estimated as:

$$P_C = ESR \cdot I^2{}_{C(rms)} \tag{17}$$

ESR stands for "equivalent series resistance" in equation (17), and $I_{C(rms)}$ stands for the maximum value of capacitor current. Similar to that, an inductor's power loss, or P_L, can be computed as:

$$P_L = r_{series} \cdot I^2{}_{L(rms)} \tag{18}$$

The series resistance of the material the inductor is built of is represented in equation (18) by r_{series}, and the maximum value of the current flowing through it is represented by $I_{L(rms)}$. As a result, the proposed converter design's overall power loss will be:

$$P_{loss} = P_S + 3P_D + P_{C1} + P_{CO} + P_{L1} + P_{L2}$$

The efficiency can be expressed as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss(total)}} \tag{19}$$

Voltage stresses

When MOSFET switch S_{W1} is kept off in Mode 2, D_{S2} turns on, and S_{W1} aligns with the load in parallel. As a result, S_{W1} is exposed to the same voltage as V_{OUT}:

$$V_{SW1(OFF)} = V_{OUT} = \frac{V_{IN}}{(1 - Dy)^2} \tag{20}$$

By applying the KVL through the loop, which is made up of D_{S3}, V_{IN}, and L_1, it is possible to determine the voltage stress over D_{S1}, $V_{D1(OFF)}$ while D_{S1} is off:

$$V_{DS1(OFF)} = V_{OUT} \cdot (2Dy - Dy^2) + V_{L1} \tag{21}$$

When D_{S2} is turned off in Mode 1, it is possible to determine the voltage stress across D_{S2}. Figure 2 demonstrates what can be seen:

$$V_{DS2(OFF)} = V_{L2(ON)} = L_2 \frac{\Delta I_{L2}}{Dy \cdot T}$$
$$V_{DS2(OFF)} = L_2 \frac{\Delta I_{L2}}{Dy} \cdot f_s \tag{22}$$

By following the KVL around the loop made up of D_{S3}, S_{W1}, and C_1 during MODE 1, the voltage stress, $V_{DS3(OFF)}$, may be determined. The voltage across D_{S3} when D_{S3} is off equals the voltage across C_1, the V_{OUT}, when S_{W1} is on. Hence:

$$V_{DS3(OFF)} = \frac{V_{IN}}{(1 - Dy)^2} \tag{23}$$

PASSIVE COMPONENTS DESIGN

Choosing the parameters of an electricity storage element is a vital part of how DC-DC converters respond and function, regardless of the topology used. Choosing the quantities of an electricity storage component is a vital part of how DC-DC converters respond and function, regardless of the topology used. As a general guideline, the inductor current's maximum ripple should not be greater than 10% of the current rating that would pass through it.

Similar to this, the maximum voltage ripple that can be tolerated by a capacitor shouldn't be higher than 10% of the highest voltage that can appear nearby. These presumptions establish a reasonable rule for determining the size of capacitors and inductive elements for a reliable structure generates a constant current and a smooth level of voltages appeared at load. The calculations used to determine the values of the capacitor and inductors employed in this suggested take into account this principle.

Design of inductors

We may use to determine the voltage that appeared across energy storage element L_1:

$$V_{IN} = L_1 . \frac{d(I_{L1})}{dt} \tag{24}$$

The change of current in the inductor L_1 is determined from above equation as:

$$\Delta I_{L1} = \frac{V_{IN} \cdot Dy \cdot T}{L_1} \tag{25}$$

The current flowing via Energy storage Element L_2 is similarly expressed as:

$$\Delta I_{L2} = \frac{V_{c2} \cdot T \cdot Dy}{L_2} \tag{26}$$

The formula for voltage appeared at capacitor C_2 found as:

$$V_{C2} = V_{IN} \frac{1}{(1 - Dy)} \tag{27}$$

From the above equation substate in V_{C2} in equation (26) we get:

$$\Delta I_{L2} = \frac{V_{in} \cdot Dy}{(1 - Dy) \cdot L_2 \cdot F_s} \tag{28}$$

From equation (25) L_1 is found as:

$$L_1 = \frac{V_{IN} \cdot Dy \cdot T}{\Delta I_{L1}} \tag{29}$$

From equation (25) find V_{in} and substate in equation (29) we get:

$$L_1 = \frac{V_{out} \cdot (1 - Dy)^2 \cdot Dy}{\Delta I_{L1} \cdot F_s} \tag{30}$$

Similarly, L_2 is:

$$L_2 = \frac{V_{out} \cdot (1 - Dy)^2 \cdot Dy}{\Delta I_{L2} \cdot (1 - Dy) \cdot F_s} \tag{31}$$

The L_1 inductor's lowest possible value is provided by the relation in equation (30). The power switch's switching frequency is F_s, the converter's output DC voltage is V_{OUT}, the ripple in inductor L_1 current is ΔI_{L1}, and duty cycle is Dy.

Design of capacitors

L_2 and C_2 are connected in series during Mode 1, and the current flowing through this branch is described as:

$$I_{C2} = C_2 \frac{d(V_{C2})}{dt} \tag{32}$$

Table 1. Ratings of design components

Components	Ratings
V_{in}	12V
R load	50 Ω
Inductors	L1 = L2 = 100 μH, ESR = 0.2 Ω
Capacitors	C1 = C2 = 150 μF, 200 V, ESR = 0.15 Ω
Diode 1 and 2	SF8L60USM
Gate drivers IC	TLP250H

Table 2. design specifications of the proposed converter

Parameter	Symbol	Value
Input voltage	V_{in}	12 V
Input current	I_{in}	53 A
Output voltage	V_o	226 V
Output current	I_o	2.62 A
Output power	P_o	592 W
Input power	P_{in}	636 W
Efficiency	η	93%
Inductor	L	100 μH
Capacitors	1C	150 μF
Duty cycle	Dy	0.75

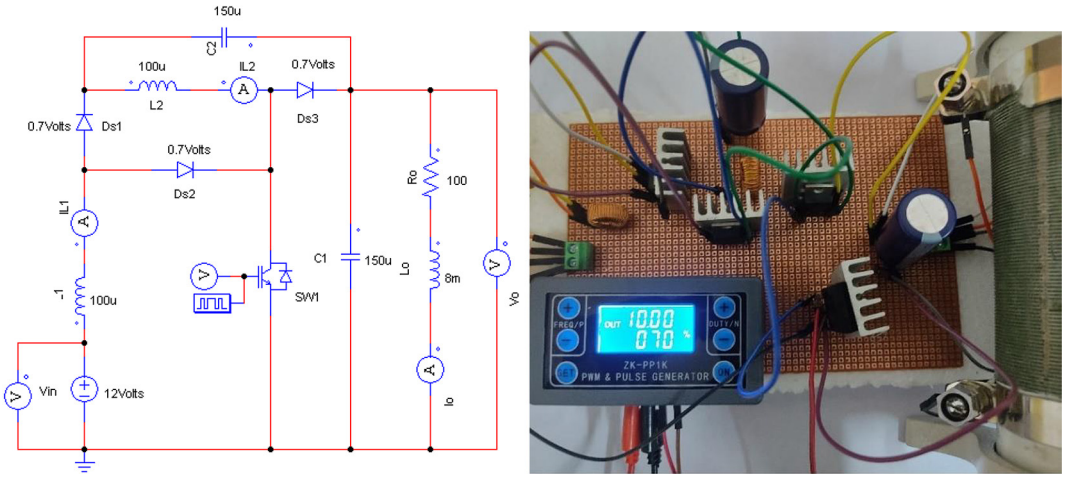

Figure 4. Simulation diagram (a) and experimental setup (b) of proposed converter

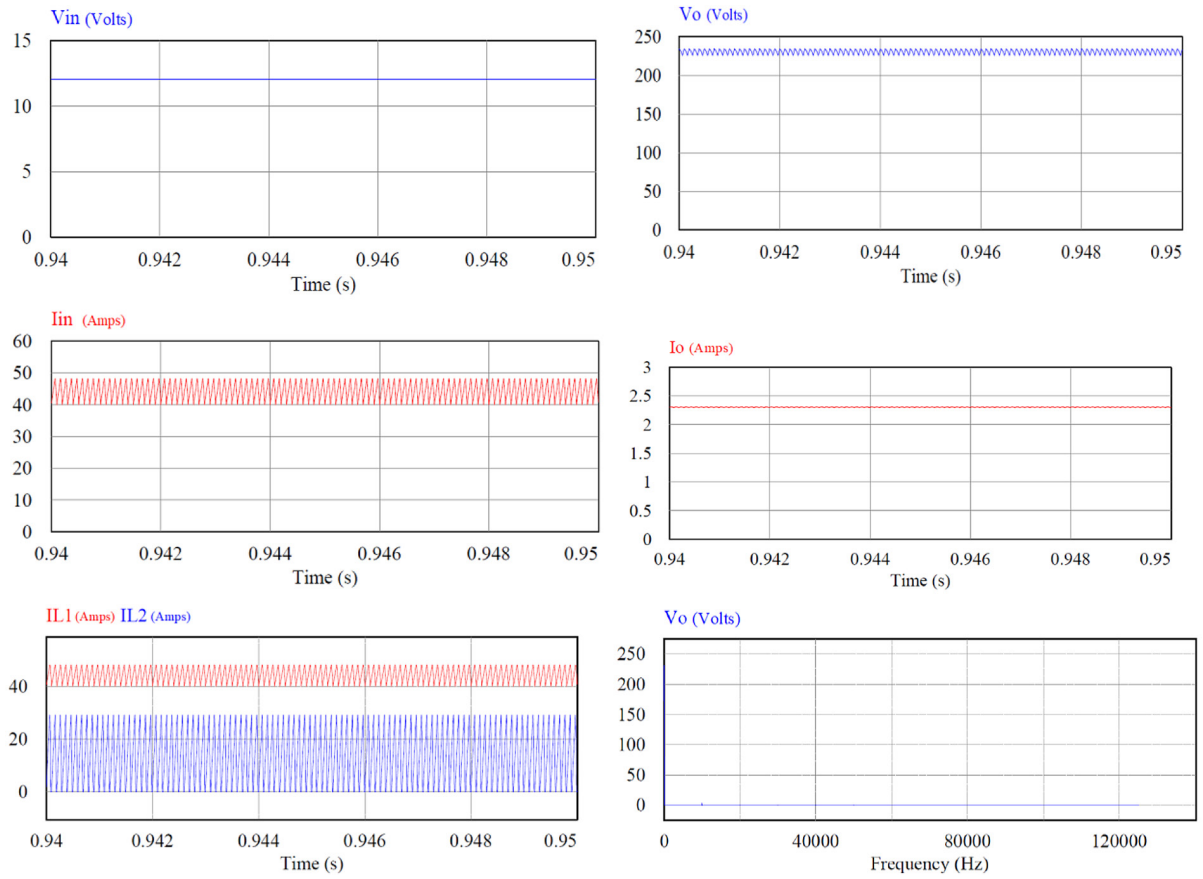

Figure 5. Simulation results of the proposed converter: (a) input voltage waveform, (b) output voltage waveform, (c) input current waveform, (d) output current waveform, (e) inductors currents waveforms, (f) FFT analysis of output voltage for 0.78 duty cycle

The equation above has the following form in Mode 1.

$$C_2 = \frac{I_1 \cdot Dy \cdot T}{\Delta V_{in}} \tag{33}$$

Substate $\Delta V_{in} = \Delta V_{C2} * (1 - Dy)$ in the above equation we get,

$$C_2 = \frac{I_1 \cdot Dy \cdot T}{\Delta V_{c1} \cdot (1 - Dy)} \tag{34}$$

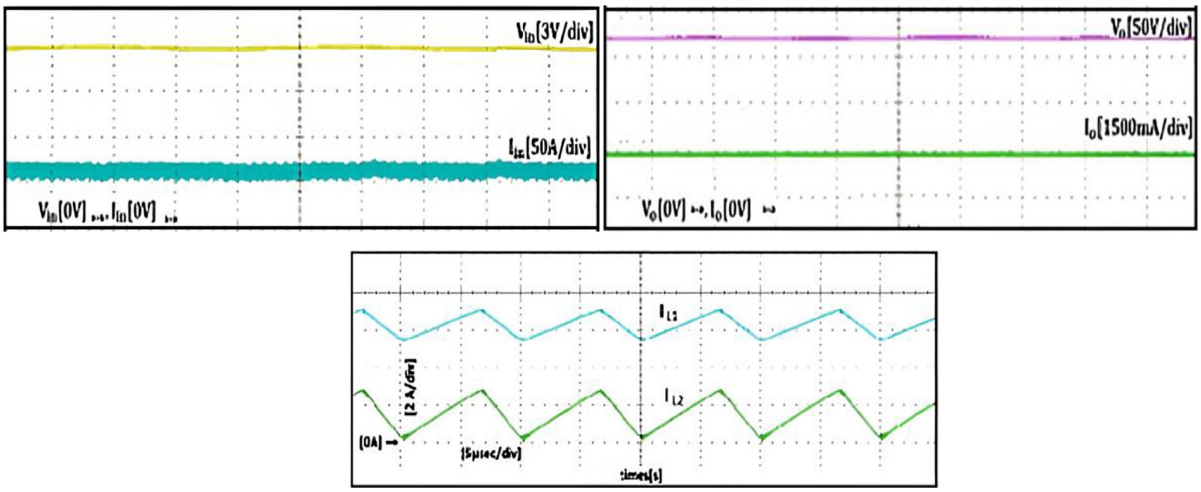

Figure 6. Experimental results of the proposed converter: (a) output voltage and output current waveforms, (b) input voltage and input current waveforms, (c) inductors current waveforms

Table 3. Voltage gains and component count analysis over several topologies

Components	Proposed in this paper	Proposed in [28]	Proposed in [29]	Proposed in [30]
Steady-state voltage gain	$\frac{1}{(1-Dy)^2}$	$\frac{1+3Dy}{(1-Dy)}$	$\frac{2}{(1-Dy)}$	$\frac{2+2Dy}{(1-Dy)}$
Number of switches	01	02	01	01
Number of inductors	02	04	01	03
Number of diodes	03	04	03	05
Number of capacitors	02	04	03	07
Number of gate drivers	01	02	01	01
Number of components	09	16	09	17
Normalized voltage stress on switches $\left(\frac{V_{sw}}{V_{IN}}\right)$	$\frac{1}{(1-Dy)^2}$	$\frac{1+3Dy}{(1-Dy)^2}$	$\frac{1}{(1-Dy)}$	$\frac{1}{(1-Dy)}$

or:

$$C_2 = \frac{I_1 \cdot Dy}{\Delta V_{c1} \cdot (1-Dy) \cdot F_s} \tag{35}$$

The equation in (35) provides the lowest value of C_2 that may be employed with ΔV_{C2} voltage ripples over C_2.

Current flow through capacitor C_1 is determined by:

$$I_{C1} = C_1 \cdot \frac{d(V_{OUT})}{dt} \tag{36}$$

During Mode 1:

$$C_1 = I_{C1} \cdot \frac{Dy}{\Delta V_{OUT} \cdot F_S} \tag{37}$$

The minimal output capacitor value with ΔV_{out} waves in the output voltage is provided by the relationship shown in (37). The duty-cycle of the converter determines the maximum limit of the output capacitor if switching frequency, output voltage ripple, and output capacitor current are all maintained constant. As a result, the output capacitor is created by running the converter at its maximum allowable duty-cycle.

RESULTS AND DISCUSSION

The suggested converter is designed to be used in a variety of applications, from hybrid cars to photovoltaic grids. These uses necessitate that the converter run in continuous-conduction mode (CCM). Even when severely loaded (R_{Load} = 5Ω), the suggested boost converter shows promising performance in CCM to maintain the steady flow of power to the load. PSIM simulation diagram of projected high voltage gain multi level DC-DC converter shown in Figure 4a.

A 500 W laboratory prototype, as seen in Fig. 4b, is used to test the theoretical analysis and the efficiency of the suggested converter while taking into account. Table 1 shows the ratings of design components and Table 2 shows the design specifications of the proposed converter.

Figure 5 shows the simulation results of the proposed converter. Figure 6 shows experimental results of the proposed converter. From these figures make it clear, that there is good agreement between the experimental and simulation results and the expected results, with an efficiency of 93%.

DC voltage gain

$$V_{out} = \frac{12}{(1 - .78)^2} = 248\ \text{V} \tag{38}$$

Its voltage gain is 19 (science it is $G = \frac{V_{OUT}}{V_{IN}}$ i.e 228/12=19).

Steady-state gain comparison among other similar converters is presented here. The step-up DC-DC converter described in [28–30] has a wide range of benefits for contemporary switching converter technology areas like renewable energy and fuel cells. According to the findings of this study, numerous voltage swing approaches can be included into this and other new federal boost converter topologies to provide high voltage boosting.

A comparison of the designs suggested in [28–30] depending on the number of switches and voltage gain. Table 3 displays the cascaded boost and the design suggested in this study. Table 1 shows that the huge high gain DC-DC converter proposed in this work has a lower component count compared to other comparable models, without a significant trade-off in DC voltage gain.

CONCLUSIONS

Comparatively speaking to several recently proposed higher voltage gain DC-DC converters, a new DC-DC boost converter with a reduction number of elements is presented in this research. For the voltage level gain, efficiency and low voltage stresses of the suggested boost converter, simulations and experimental results are validated the proposed design's viability.

Based on number of elements and component sizing, a 500 Watts sample model was simulated and designed. The outcomes were then compared with existing boost converter models. The comparison made it abundantly evident that the proposed design effectively achieved high-voltage gain while minimizing the number of components without compromising efficiency and extreme duty cycle. But the maximum voltage stresses across the switch and diodes are higher in comparison to the other converters.

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